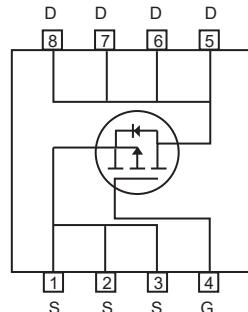
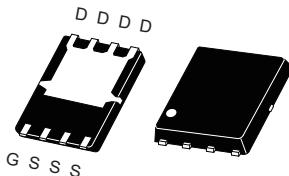


P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- -100V, -28A, $R_{DS(ON)} = 55 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$.
 $R_{DS(ON)} = 60 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Surface mount Package.



P-PAK 5X6

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units	
Drain-Source Voltage	V_{DS}	-100	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Drain Current-Continuous	$I_D @ R_{\theta JC}$	$T_C = 25^\circ\text{C}$	-28	A
		$T_C = 70^\circ\text{C}$	-22	A
	$I_D @ R_{\theta JA}$	$T_A = 25^\circ\text{C}$	-8	A
		$T_A = 70^\circ\text{C}$	-6	A
Drain Current-Pulsed ^a	$I_{DM} @ R_{\theta JC}$	$T_C = 25^\circ\text{C}$	-112	A
	$I_{DM} @ R_{\theta JA}$	$T_A = 25^\circ\text{C}$	-32	A
Maximum Power Dissipation	P_D	73	W	
Single Pulsed Avalanche Energy ^d	E_{AS}	200	mJ	
Single Pulsed Avalanche Current ^d	I_{AS}	20	A	
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$	

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.7	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	20	$^\circ\text{C}/\text{W}$

This is preliminary information on a new product in development now
Details are subject to change without notice .

Rev 1. 2024.July
<http://www.cet-mos.com>



CEZ3010P

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -100\text{V}, V_{\text{GS}} = 0\text{V}$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = -250\mu\text{A}$	-1		-3	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -16\text{A}$		44	55	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -8\text{A}$		48	60	$\text{m}\Omega$
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{\text{DS}} = -25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		4340		pF
Output Capacitance	C_{oss}			215		pF
Reverse Transfer Capacitance	C_{rss}			175		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = -50\text{V}, I_D = -18\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GEN}} = 3.3\Omega$		20		ns
Turn-On Rise Time	t_r			9		ns
Turn-Off Delay Time	$t_{\text{d(off)}}$			85		ns
Turn-Off Fall Time	t_f			17		ns
Total Gate Charge	Q_g	$V_{\text{DD}} = -80\text{V}, I_D = -18\text{A}, V_{\text{GS}} = -4.5\text{V}$		44		nC
Gate-Source Charge	Q_{gs}			8		nC
Gate-Drain Charge	Q_{gd}			22		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S				-28	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_S = -16\text{A}$			-1.2	V
Notes :						
a.Repetitive Rating : Pulse width limited by maximum junction temperature.						
b.Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.						
c.Guaranteed by design, not subject to production testing.						
d.L = 1mH, $I_{AS} = 20\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.						

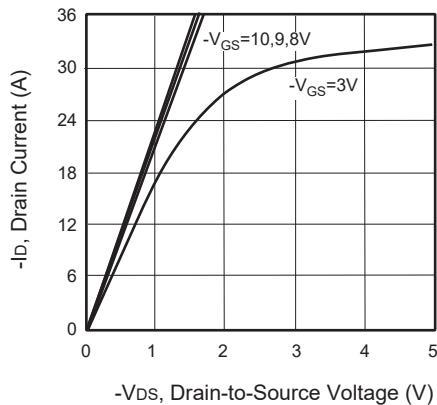


Figure 1. Output Characteristics

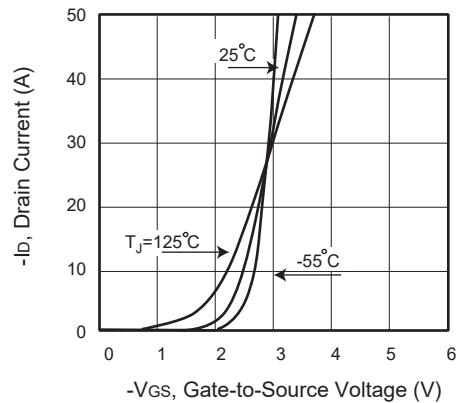


Figure 2. Transfer Characteristics

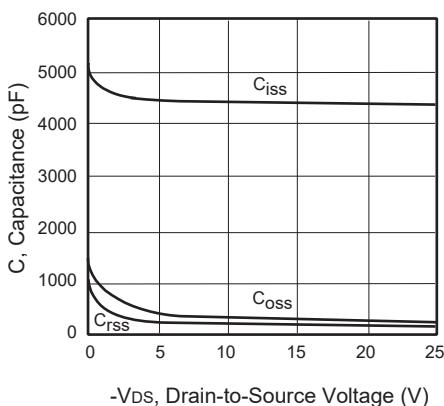


Figure 3. Capacitance

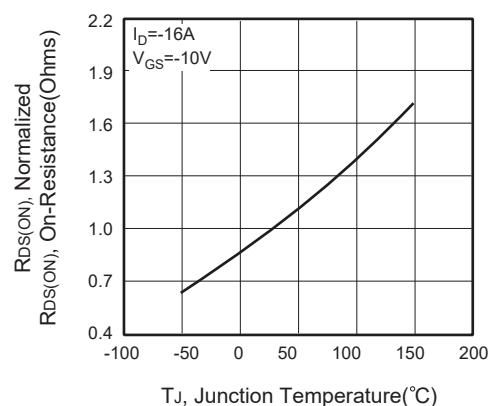


Figure 4. On-Resistance Variation with Temperature

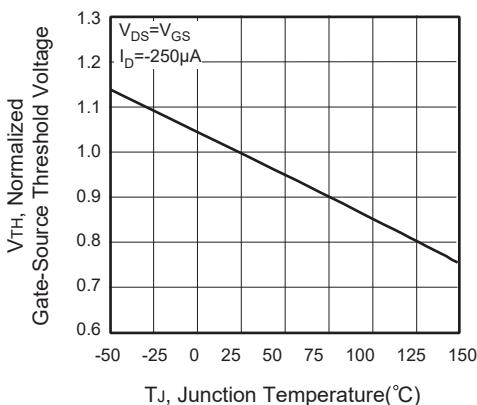


Figure 5. Gate Threshold Variation with Temperature

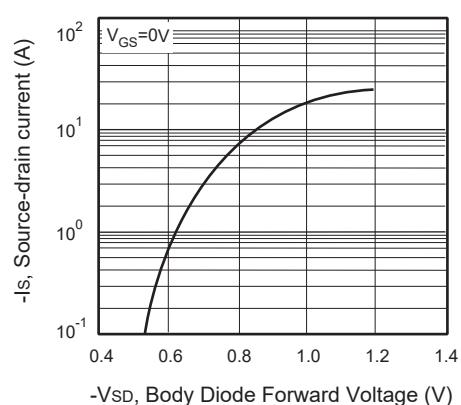
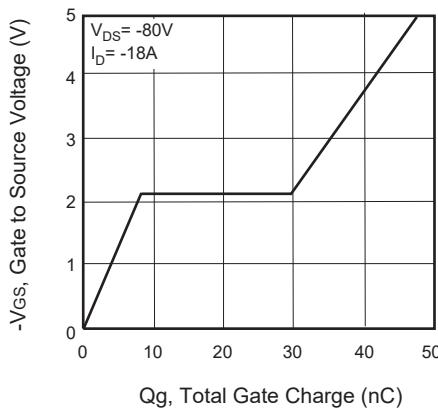
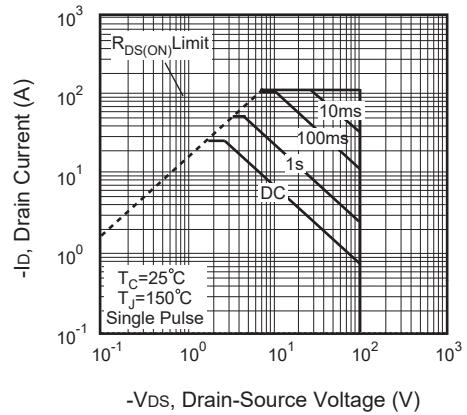


Figure 6. Body Diode Forward Voltage Variation with Source Current



Qg, Total Gate Charge (nC)

Figure 7. Gate Charge



$-V_{DS}$, Drain-Source Voltage (V)

Figure 8. Maximum Safe Operating Area

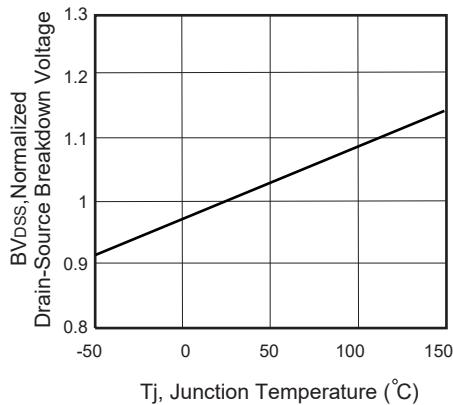


Figure 9. Breakdown Voltage Variation VS Temperature

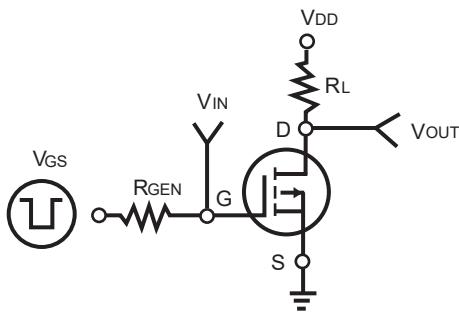


Figure 10. Switching Test Circuit

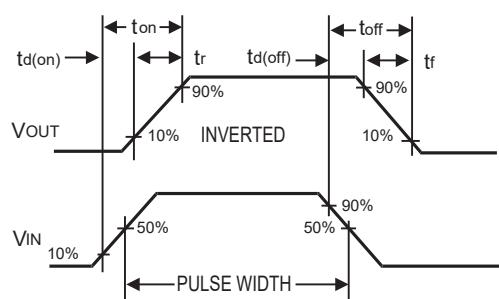
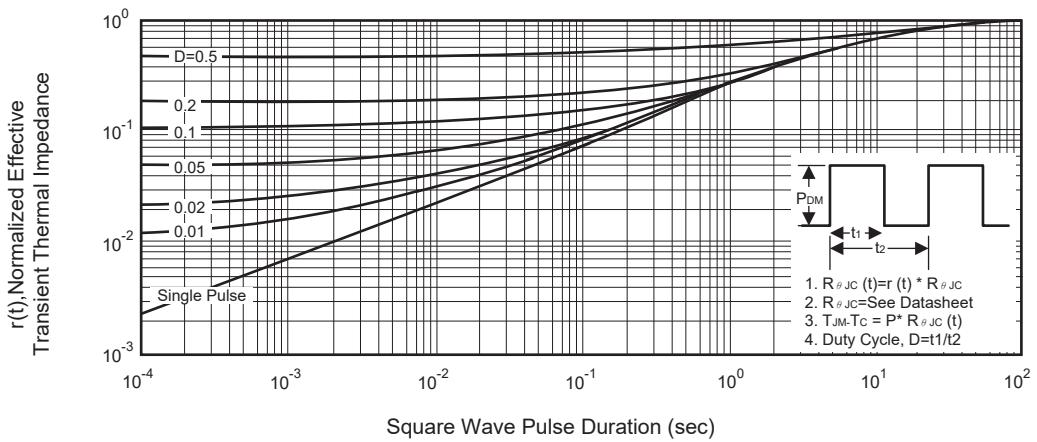


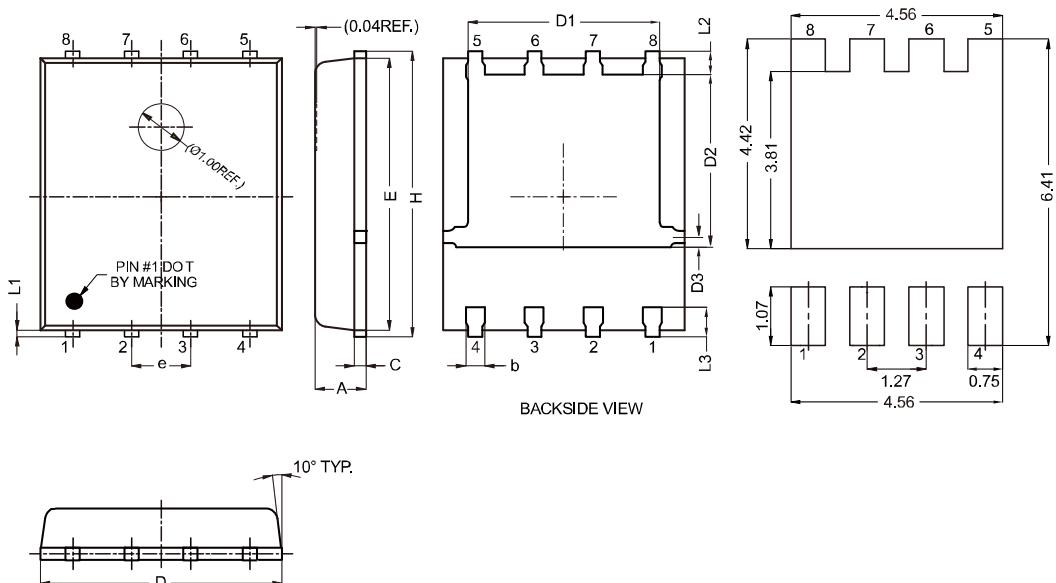
Figure 11. Switching Waveforms

**Figure 11. Normalized Thermal Transient Impedance Curve**

P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)

SINGLE PAD 尺寸圖

Land Pattern
(Only for Reference)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.154	0.354	0.006	0.014
D	5.000	5.400	0.197	0.213
D1	3.800	4.250	0.150	0.167
D2	3.570	3.970	0.141	0.156
D3	0.380	0.850	0.015	0.033
E	5.660	6.060	0.223	0.239
e	1.270 TYP		0.050 TYP	
H	5.950	6.350	0.234	0.250
L1	0.080	0.330	0.003	0.013
L2	0.400	0.600	0.016	0.024
L3	0.500	0.700	0.020	0.028